a gate formed above the semiconductor substrate;

C1 Cont.

an isolation region located within a trench formed in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions;

a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(2) Kindly rewrite Claim 7 as follows:

7. (Thrice Amended) A semiconductor device, comprising:

C2

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation region located in the trench, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions; and

a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(3) Kindly rewrite Claim 12 as follows:

12. (Thrice Amended) A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

C3

an isolation region located adjacent the channel region, the isolation region being located within a trench formed in the semiconductor substrate and not extending under the channel region and including a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions; and

source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region and in contact with the second post portion, but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(4) Kindly rewrite Claim 17 as follows:

17. (Thrice Amended) A semiconductor device, comprising:

C4

a first transistor located adjacent a second transistor, wherein both the first and second transistors are located over a semiconductor substrate;

an isolation region located between the first and second transistors and within a trench located within the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions; and

source/drain regions associated with each of the first and second transistors, each of the source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region and in contact with the second post portion, but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(5) Kindly rewrite Claim 21 as follows:

21. (Thrice Amended) A method of manufacturing a semiconductor device, comprising:

C5

providing a semiconductor substrate;

creating a gate above the semiconductor substrate;

forming an isolation region within a trench located in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions;

forming a first portion of one of a source/drain region in the semiconductor substrate and a second portion of the one of the source/drain region on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(6) Kindly rewrite Claim 27 as follows:

27. (Thrice Amended) An integrated circuit, comprising:

C6

semiconductor devices, including;

a semiconductor substrate;

a gate formed above the semiconductor substrate;

an isolation region located within a trench formed in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions;